What is claimed is:

1. A method for debugging an SoC having at least one functional block, each of said functional blocks being controlled by a block clock and at least one of said functional blocks having at least one scan chain, the method comprising the steps of:

recognizing activation of a debug trigger signal;

halting each block clock;

selecting from said at least one scan chain, a selected scan chain containing at least one register element;

providing control of the selected scan chain to a scan clock signal;

shifting out the contents of said at least one register element in the selected scan chain; and,

utilizing said contents to debug the SoC.

2. The method of claim 1 further comprising the step of recognizing a debug ack signal inputted by a user.

3. The method of claim 2 further comprising the steps of:

determining that the debug trigger signal is held active after said shifting step is completed;

permitting the user to identify a subsequent scan chain;

repeating said configuring, providing, shifting and utilizing steps using said subsequent scan chain as the selected scan chain.

4. The method of claim 1 further comprising the steps of :

recognizing the deactivation of the debug trigger signal; and,

returning each block clock to its operative state.

5. The method of claim 4 further comprising a step of configuring each of the at least one register elements in said selected scan chain with test values, wherein said configuring step occurs previous in time to said recognizing and said returning steps.

6. The method of claim 1 wherein the SoC comprises cells containing nonscan flip-flops, the method further comprising the step of disabling all clocks to said cells while said debug trigger signal is active.

7. The method of claim 1 wherein the SoC contains at least one device controlling a bidirectional data bus, the method further comprising the step of disabling said devices while said debug trigger signal is active.

8. An apparatus for debugging an SoC having at least one functional block, each of said functional blocks being controlled by a block clock and at least one of said functional blocks having at least one scan chain, the apparatus comprising:

means for recognizing the activation of a debug trigger signal;

means for halting each block clock;

means for selecting from said at least one scan chain, a selected scan chain, said scan chain containing at least one register element;

means for providing control of the scan chain to a scan clock signal;

means for shifting out the contents of said at least one register element in the selected scan chain; and,

means for utilizing said contents to debug the SoC.

9. The apparatus of claim 8 further comprising a means for recognizing a debug ack signal inputted by a user.

10. The apparatus of claim 9 further comprising:

means for determining that the debug trigger signal is held active after said scan chain contents have been shifted out;

means for permitting the user to identify a subsequent scan chain;

means for repeating said configuring, providing, shifting and utilizing operations using said subsequent scan chain as the selected scan chain.

11. The apparatus of claim 8 further comprising:

means for recognizing the deactivation of the debug trigger signal; and,

means for returning each block clock to its operative state.

12. The apparatus of claim 11 further comprising a means for configuring each of the at least one register elements in said selected scan chain with test values, wherein said configuring occurs previous in time to invoking said means for recognizing and said means for returning.

13. The apparatus of claim 8 wherein the SoC comprises cells containing nonscan flip-flops, the apparatus further comprising a means for disabling all clocks to said cells while said debug trigger signal is active.

14. The apparatus of claim 8 wherein the SoC contains at least one device controlling a bidirectional data bus, the apparatus further comprising a means for disabling said devices while said debug trigger signal is active.

15. The apparatus of claim 8 wherein said means for utilizing comprises a computer.

16. The apparatus of claim 15 wherein said computer is at a location remote from the SoC.

17. The apparatus of claim 15 wherein said computer comprises a means for automatically debugging said SoC.

18. The apparatus of claim 15 wherein said means for utilizing further comprises:

a means for running a software model of the SoC to yield expected system content values; and,

a means for comparing said expected system content values with the scan contents.

19. A data storage media comprising indicia of instructions for a processor to perform a method of debugging a SoC, said SoC having at least one functional block, each of said functional blocks being controlled by a block clock and at least one of said functional blocks having at least one scan chain, the method comprising the steps of:

recognizing activation of a debug trigger signal;

halting each block clock;

selecting from said at least one scan chain, a selected scan chain containing at least one register element;

providing control of the selected scan chain to a scan clock signal;

shifting out the contents of said at least one register element in the selected scan chain; and,

utilizing said contents to debug the SoC.